IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**BRUIN**
Application No.	:	**10/531,603**
Filed	:	**14/14/2005**
For	:	**FREQUENCY-INDEPENDENT VOLTAGE DIVIDER**

APPEAL BRIEF

On Appeal from Group Art Unit 2816

Date: 07/16/2007

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Michael Ure
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8/15/07
(Signature and Date)

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TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-6 are pending, of which claims 1-5 stand finally rejected and form the subject matter of the present appeal. Claim 6 has been objected to. Claim 7 has been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a compensation arrangement that compensates for the parasitic capacitance of an integrated resistor forming part of a voltage divider, the

resistor having a meandering shape, for example. In contrast to the prior art (Fig. 3 of the present application) in which a compensation structure is formed above the resistor, in the case of the present invention (Fig. 4), the compensation structure is formed beneath the resistor and is separated from the resistor and from the substrate by insulating layers. By forming the compensation structure between the substrate and resistor, the resistor is partially shielded from the substrate, which has been found to enable more accurate compensation.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A voltage divider arrangement comprising	Fig. 6	Page 5, lines 11-16
a reference terminal (1),	Fig. 6, 1	Page 5, lines 11-16
an input terminal (2) for receiving an input signal with respect to said reference terminal (1),	Fig. 6, 2	Page 5, lines 11-16
an output terminal (3) for supplying an output signal with respect to said reference terminal (1), and	Fig. 6, 3	Page 5, lines 11-16
a resistor arrangement (20) arranged on a substrate (50) and coupled between said input terminal (2) and said reference terminal (1),	Fig. 6, 20	Page 5, lines 11-16
wherein a distributed compensation capacitance structure (10) for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement (20) and said substrate (50);	Fig. 6, 10	Page 5, lines 11-16
wherein said distributed compensation capacitance	Fig. 4: 10, 30, 40	Page 4, lines 10-19

structure (10) is separated from said resistor arrangement (20) and said substrate (50) by respective insulation layers (30, 40).		

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102(a), claims 1, 2 and 4 are anticipated by Hojabri.
2. under 35 USC 103(a), claims 1-5 and 7 are unpatentable over Van Der Zee in view of Bucksch.

VII. ARGUMENT

I. Rejection of Claims 1, 2 and 4 as Anticipated by Hojabri

Hojabri relates to a structure for compensating for the parasitic capacitance of the resistor of an integrator. The integrator is shown in Figure 5 of Hojabri, wherein the resistor is *modeled* as a pi network 500 (Hojabri, col. 5, lines 22-25). A compensation capacitor C_C is formed as shown in Figure 6 of Hojabri. In particular, the compensation capacitor is formed in similar manner as an integrated resistor, by a polysilicon meander line 604 insulated by silicon dioxide 602. The compensation capacitor is formed within an n-well, which serves as the bottom plate of the capacitor, opposite the meander line. Unlike a resistor, however, to form the compensation capacitor, the ends of the meander line are shorted together to form the top plate of the compensation capacitor.

Several important differences distinguish the invention of claim 1 from Hojabri. First, Hojabri does not show a voltage divider arrangement as claimed. (Recall that the pi network 500 of Figure 5 of Hojabri is in fact a single resistor.) What Hojabri shows, therefore, is either an integrator arrangement considering the whole of Figure 5 or, considering only a portion of Figure 5, a resistor arrangement.

Second, Hojabri does not show a distributed compensation capacitance structure arranged between a resistor arrangement and the substrate. The compensation capacitance structure is not arranged between the resistor arrangement 500 and the substrate, as the resistor arrangement 500 and the compensation capacitance structure are formed in separate wells to avoid noise coupling (Hojabri, col. 5, lines 50-60). Moreover, although the compensation capacitance structure of Figure 6 has in part a similar form as a resistor arrangement, it is clearly not a resistor arrangement as should be clear from the fact that

the ends of the meander line are shorted together. Rather, it is (indisputably) a capacitor having a meander line structure.

Accordingly, Hojabri does not anticipate claim 1 or its dependent claims 2 and 4.

II. Rejection of Claims 1-5 and 7 as Unpatentable Over Van Der Zee in View of Bucksch

Van Der Zee discloses a voltage divider arrangement like that of prior art Figure 3 of the present application.

Bucksch discloses a voltage divider arrangement in which stray capacitance compensation is achieved through a combination of suitable dimensioning of resistor paths and by connection of the input and reference terminals to respective wells in which partial resistors R1 and R2 are formed.

Bucksch does not teach the use of a layer compensation capacitance structure (4) for compensating the influence of a distributed parasitic capacitance arranged between a resistor arrangement and a substrate. The layer 4 of Bucksch is merely an insulating layer for insulating the resistors from the underlying wells in which they are formed. This necessary insulating layer forms part of the stray capacitance of the resistors (Bucksch, col. 3, lines 6-12). It in no way performs any compensation function.

In fact, the layer 4 of Bucksch corresponds exactly to the isolator I of Figure 3 of Van Der Zee (col. 3, line 66 to col. 4, line 16). Hence, the combination of Bucksch with Van Der Zee yields nothing more than Van Der Zee itself.

Accordingly, claim 1 is believed to patentably define over the cited references. Claims 2-5 are also believed to add novel and patentable subject matter to independent

claim 1. In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 8/15/07

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A voltage divider arrangement comprising a reference terminal (1), an input terminal (2) for receiving an input signal with respect to said reference terminal (1), an output terminal (3) for supplying an output signal with respect to said reference terminal (1), and a resistor arrangement (20) arranged on a substrate (50) and coupled between said input terminal 2) and said reference terminal (1), wherein a distributed compensation capacitance structure (10) for compensating the influence of a distributed parasitic capacitance is arranged between said resistor arrangement (20) and said substrate (50); wherein said distributed compensation capacitance structure (10) is separated from said resistor arrangement (20) and said substrate (50) by respective insulation layers (30, 40).

2. A voltage divider arrangement according to claim 1, wherein said resistor arrangement (20) has a meandering shape.

3. A voltage divider arrangement according to claim 2, wherein said resistor arrangement (20) is made of polysilicon.

4. A voltage divider arrangement according to claim 1, wherein said distributed compensation capacitance structure (10) comprises a conductor layer of a predetermined shape.

5. A voltage divider arrangement according to claim 4, wherein said predetermined shape is a triangular shape.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE